CLAIMS

What is claimed is:

1. A reference cell for determining a state stored in a first memory cell, comprising:

a second memory cell that produces a current; and

a current reduction element that

is coupled to the memory cell,

is configured to receive a reference voltage, and

has a resistance that varies as a function of the reference voltage.

2. The reference cell of claim 1, wherein the second memory cell is a TCCT based memory cell.

3. The reference cell of claim 1, wherein the second memory cell is an SRAM memory cell.

4. The reference cell of claim 1, wherein the second memory cell is an MRAM memory cell.

5. The reference cell of claim 1, wherein the second memory cell is a memory cell with a floating gate.

6. The reference cell of claim 1, wherein the current reduction element is a transistor.

7. A reference cell for a TCCT based memory cell, comprising:

an NDR device including

a first end configured to have a first voltage applied thereto,

a second end,

a doped semiconductor layer between the first and second ends, and

a gate-like device disposed adjacent to the doped semiconductor layer;

a first word line;

a second word line coupled to the gate-like device;

a pass transistor including

a drain,

a source coupled to the second end, and

a gate coupled to the first word line;

a bit line; and

a current reduction element coupled between the bit line and the drain.

8. The reference cell of claim 7 wherein the current reduction element is a second pass transistor including a gate having a second voltage applied thereto.

9. A circuit to generate a reference voltage, comprising:

a memory cell configured to generate a first current;

a reference cell configured to generate a second current; and

a feedback circuit configured to

compare the first current to the second current, and

generate a reference voltage in response thereto.

10. The circuit of claim 9 wherein the reference cell is configured to receive the reference voltage.

11. The circuit of claim 10 wherein the second current varies as a function of the reference voltage.

12. The circuit of claim 11 wherein the reference cell includes a pass transistor configured to receive the reference voltage.

13. The circuit of claim 12 wherein the memory cell includes a pass transistor having a first W/L ratio.

14. The circuit of claim 13 wherein the pass transistor of the reference cell has a second W/L ratio equal to about twice the first W/L ratio.

15. A circuit to generate a reference voltage, comprising:

a memory cell configured to generate a first current;

a first reference cell configured to generate a second current;

a second reference cell configured to generate a third current; and

a feedback circuit configured to

compare the first current to the sum of the second and third currents, and

generate a reference voltage in response thereto.

16. The circuit of claim 15 wherein the first and second reference cells are each configured to receive the reference voltage.

17. The circuit of claim 16 wherein the second and third currents vary as a function of the reference voltage.

18. The circuit of claim 15 wherein the memory cell is a TCCT based memory cell and includes an NDR device coupled to a first pass transistor.

19. The circuit of claim 15 wherein multiple memory cells generate the first current, multiple first reference cells generate the second current, and multiple second reference cells generate the third current.

20. The circuit of claim 15 wherein the first and second reference cells each include

an NDR device,

a first pass transistor coupled to the NDR device, and

a second pass transistor coupled to the first pass transistor.

21. The circuit of claim 20 wherein each second pass transistor has a gate configured to receive the reference voltage.

22. The circuit of claim 21 wherein the feedback circuit maintains the sum of the second and third currents equal to the first current by adjusting the reference voltage.

23. The circuit of claim 15 wherein the feedback circuit includes a current comparator coupled to a ramp output voltage generator.

24. The circuit of claim 15 wherein the memory cell is an SRAM cell that includes a pass transistor.

25. The circuit of claim 15 wherein the memory cell is a floating gate based memory cell that includes a pass transistor.

26. The circuit of claim 15 wherein the memory cell is an MRAM cell that includes a pass transistor.

27. A circuit to generate a reference voltage to control a current output of a reference cell, comprising:

a TCCT based memory cell including an NDR device and configured to generate a first current;

a first reference cell configured to generate a second current and including an NDR device, and a pass transistor coupled to the NDR device;

a second reference cell configured to generate a third current and including an NDR device, and a pass transistor coupled to the NDR device; and

a feedback circuit configured to compare the first current to the sum of the second and third currents, and generate a reference voltage in response thereto.

28. The circuit of claim 27 wherein the pass transistors of the first and second reference cells each have a gate configured to receive the reference voltage.

29. The circuit of claim 28 wherein the feedback circuit maintains the sum of the second and third currents equal to the first current by adjusting the reference voltage.

30. The circuit of claim 29 wherein the feedback circuit maintains the sum of the currents from more than two memory elements equal to the first current by adjusting the reference voltage.

31. The circuit of claim 27 wherein the feedback circuit includes a current comparator coupled to a ramp output voltage generator.

32. A memory array comprising:

a memory cell having a state and configured to generate a first current on a first bit line;

a circuit configured to generate a reference voltage;

a reference cell configured to receive the reference voltage and to generate a second current on a second bit line; and

means for determining the state of the memory cell by comparing the first current to the second current.

33. The memory array of claim 32 wherein the memory array further comprises first and second word lines and the memory cell is a TCCT based memory cell including

a first NDR device disposed adjacent to the second word line, and

a first pass transistor with a gate coupled to the first word line.

34. The memory array of claim 32 wherein the reference cell includes

an NDR device disposed adjacent to the second word line, and

a pass transistor having a gate with the reference voltage applied thereto.

35. The memory array of claim 32 wherein the means for determining a state of the TCCT based memory cell is a sense amplifier.

36. The memory array of claim 32 wherein the memory cell is an SRAM memory cell and the means for determining a state of the SRAM cell is a sense amplifier.

37. The memory array of claim 32 wherein the memory cell is an MRAM memory cell and the means for determining a state of the MRAM cell is a sense amplifier.

38. The memory array of claim 32 wherein the memory cell is a memory cell with a floating gate and the means for determining a state of the memory cell with a floating gate is a sense amplifier.

39. A memory array comprising:

a first bit line;

a second bit line;

a first word line;

a second word line;

a TCCT based memory cell including

a first NDR device disposed adjacent to the second word line and having

a first end having a first voltage applied thereto, and

a second end;

a first pass transistor having

a source coupled to the second end of the first NDR device,

a drain coupled to the first bit line, and

a gate coupled to the first word line; and

a reference cell including

a second NDR device disposed adjacent to the second word line and having

a first end having the first voltage applied thereto, and

a second end;

a second pass transistor having

a source coupled to the second end of the second NDR device,

a drain, and

a gate coupled to the first word line;

a current reduction element coupled between the second bit line and the drain of the second pass transistor; and

means for determining a state of the TCCT based memory cell by comparing a first current on the first bit line and a second current on the second bit line.

40. The memory array of claim 39 wherein the means for determining a state of the TCCT based memory cell is a sense amplifier.

41. The memory array of claim 39 further including a circuit to generate a reference voltage to control the second current.

42. The memory array of claim 41 wherein the reference voltage is applied to the current reduction element.

43. The memory array of claim 42 wherein the current reduction element is a third pass transistor.

44. A memory device, comprising:

at least one memory array including

at least one TCCT based memory cell;

at least one reference cell; and

a sense amplifier configured to

receive a memory cell current produced by the at least one TCCT based memory cell,

receive a reference cell current produced by the at least one reference cell, and

compare the memory cell current with the reference cell current to determine a state of the at least one TCCT based memory cell.

45. A method for producing a reference current, comprising:

providing a reference cell including

an NDR device configured to produce a current, and

a pass transistor connected to the NDR device and having a gate;

providing a circuit configured to produce a reference voltage; and

applying the reference voltage to the gate.

46. The method of claim 45 wherein providing a circuit includes

providing a memory cell producing a first current;

providing a first circuit reference cell producing a second current;

providing a second circuit reference cell producing a third current; and

comparing the first current with the sum of the second and third currents.

47. The method of claim 46 wherein providing a circuit further includes applying the reference voltage to the first and second circuit reference cells.

48. The method of claim 47 wherein providing a circuit further includes adjusting the reference voltage to maintain the sum of the second and third currents equal to the first current.

49. A method for producing a reference current for determining a state of a TCCT based memory cell, comprising:

generating a first current by a first TCCT based memory cell; and

adjusting the first current to produce the reference current.

50. The method of claim 49 wherein adjusting the first current includes generating a reference voltage.

51. The method of claim 50 wherein generating the reference voltage includes

generating a second current by a second TCCT based memory cell,

generating a third current by a third TCCT based memory cell, and

comparing the second current to the third current.

52. The method of claim 51 wherein the third current varies a function of the reference voltage.

53. The method of claim 52 wherein comparing the second current to the third current includes

determining whether the third current is about half of the second current.

54. The method of claim 53 wherein determining whether the third current is about half of the second current includes

generating a fourth current by a fourth TCCT based memory cell wherein the fourth current varies a function of the reference voltage and is substantially the same as the third current, and

comparing the sum of the third and fourth currents to the second current.

55. A method for reading a state of a memory cell, comprising:

operating the memory cell to produce a first current on a first bit line;

operating a reference cell to produce a second current on a second bit line;

operating a circuit to provide a reference voltage to the reference cell; and

comparing the first and second currents to determine the state of the memory cell.

56. The method of claim 55 wherein the memory cell is a TCCT based memory cell and operating the memory cell includes applying a first voltage to one end of the TCCT based memory cell.

57. The method of claim 56 wherein operating the memory cell further includes applying a second voltage to a gate of a pass transistor of the TCCT based memory cell.

58. The method of claim 55 wherein operating the reference cell includes applying a first voltage to one end of the reference cell.

59. The method of claim 58 wherein operating the reference cell further includes applying a second voltage to a gate of a pass transistor of the reference cell.

60. The method of claim 59 wherein the second voltage is the reference voltage.

61. The method of claim 55 wherein operating the circuit includes

operating a circuit memory cell configured to produce a third current;

operating a circuit reference cell configured to produce a fourth current; and

using a feedback circuit configured to

receive the third and fourth currents,

provide the reference voltage to the circuit reference cell, and

adjust the reference voltage such that the fourth current is about half of the third current.